FIG.1

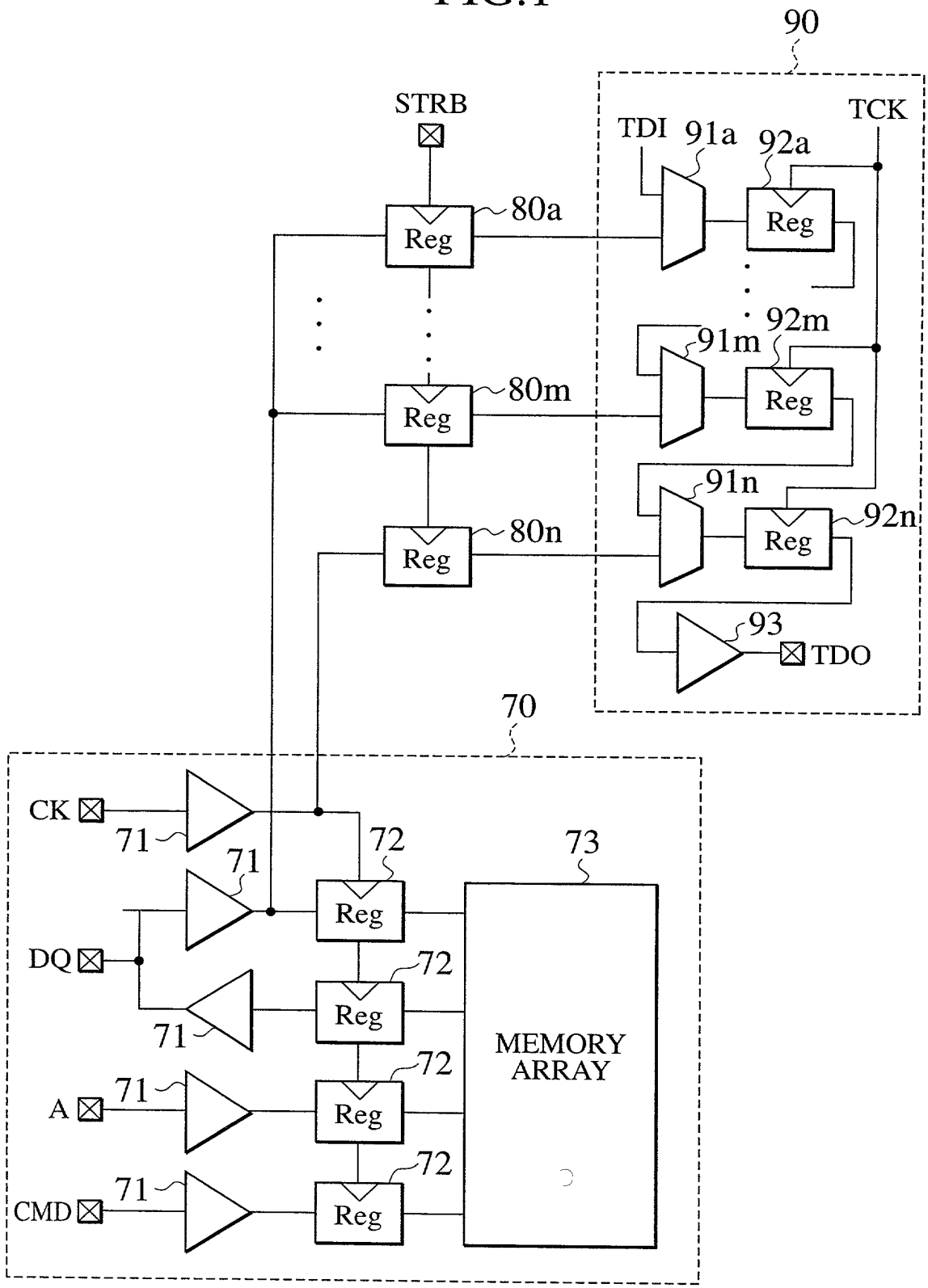

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FIG.2A

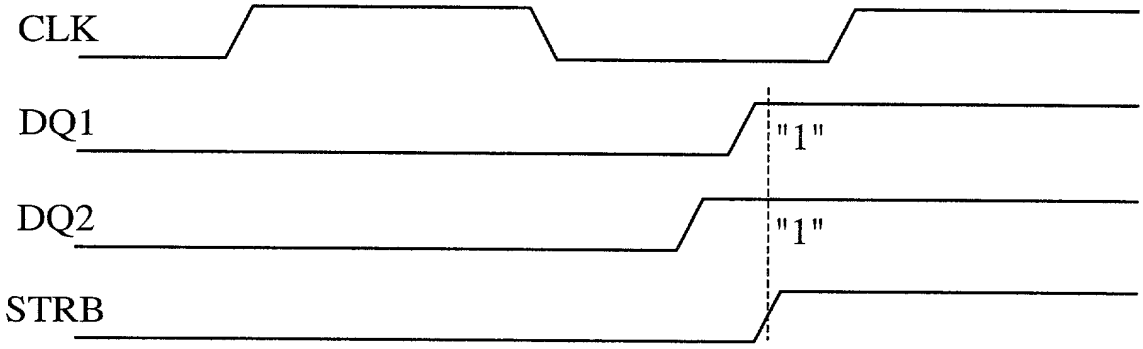

FIG.2B

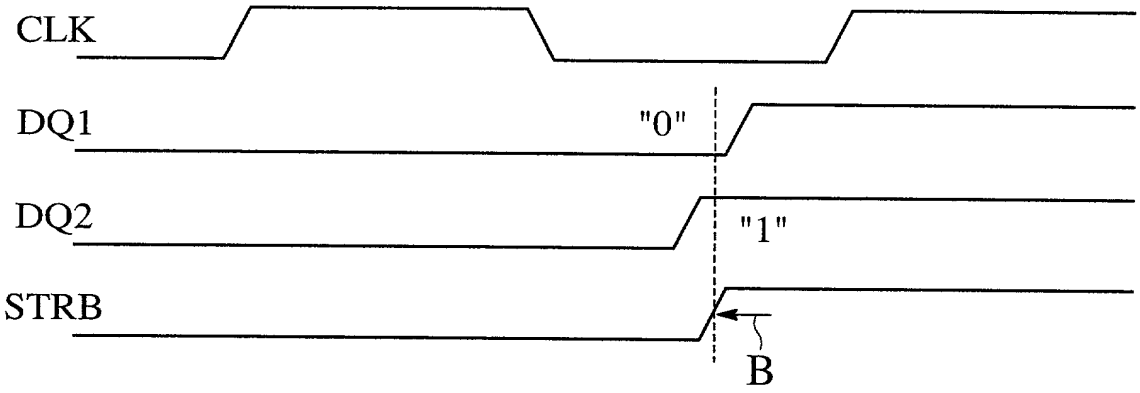

FIG.2C

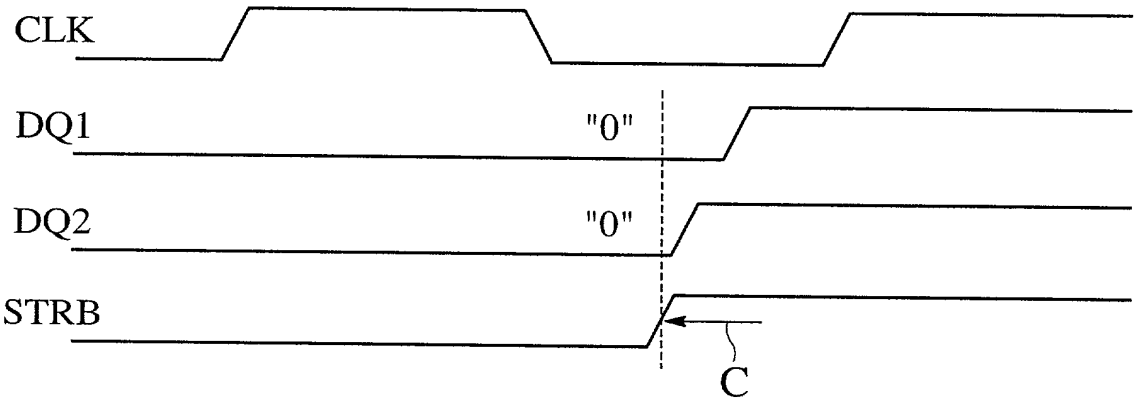

FIG.3

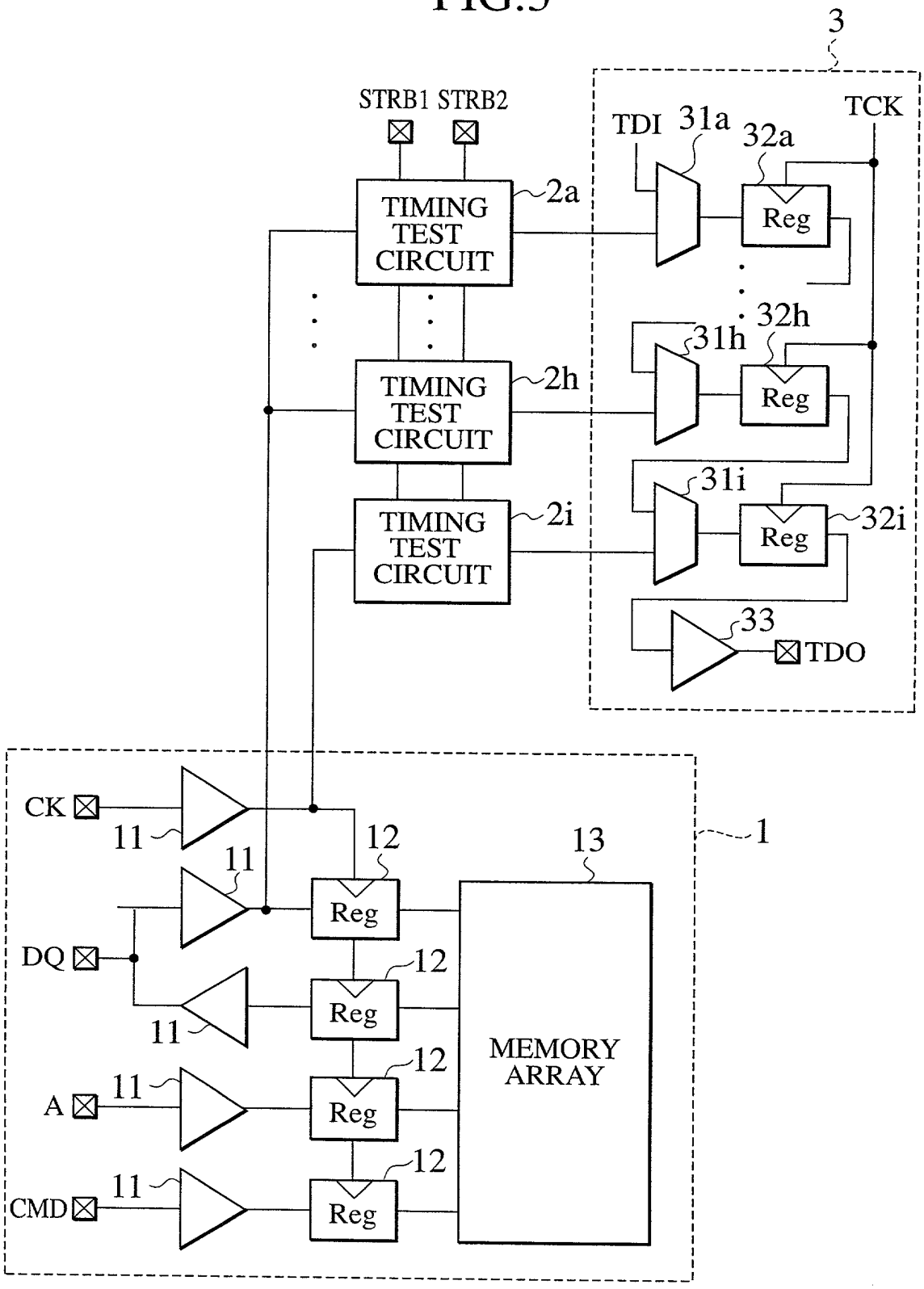
3
STRB1
STRB2
TDI
31a
32a
TCK
TIMING TEST CIRCUIT
2a
Reg
32h
31h
2h
31i
2i
32i
33
TDO
CK
11
12
13
1
DQ
MEMORY ARRAY
A
CMD

FIG.4

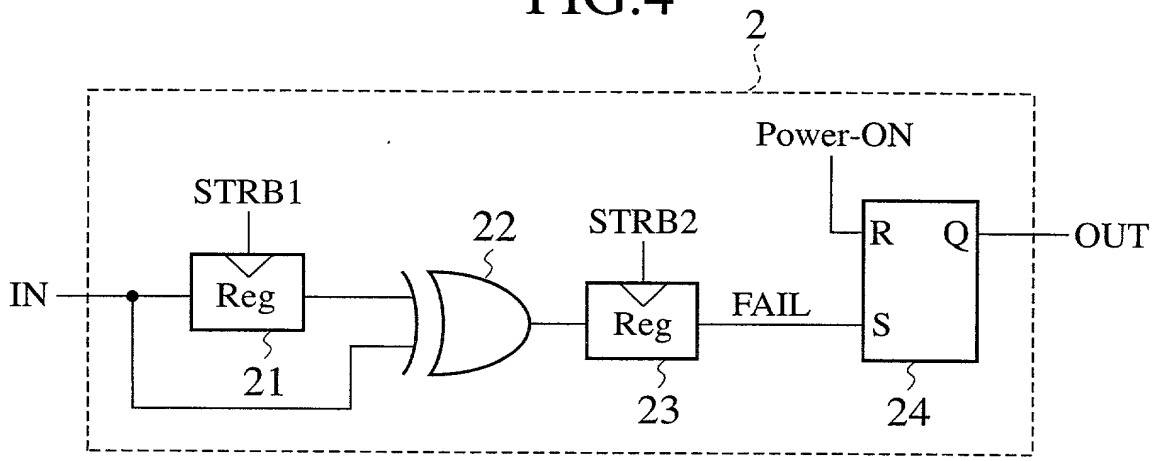
2
Power-ON
STRB1
22
STRB2
R
Q
OUT
IN
Reg
FAIL
S
21
23
24

FIG.5

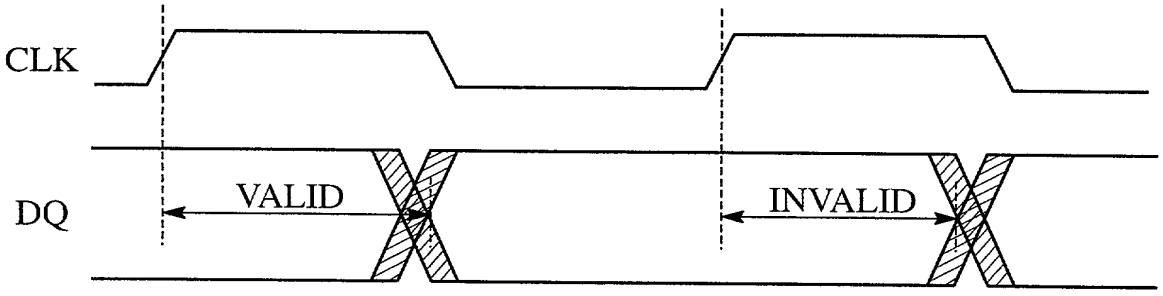
CLK
DQ
VALID
INVALID

FIG.6

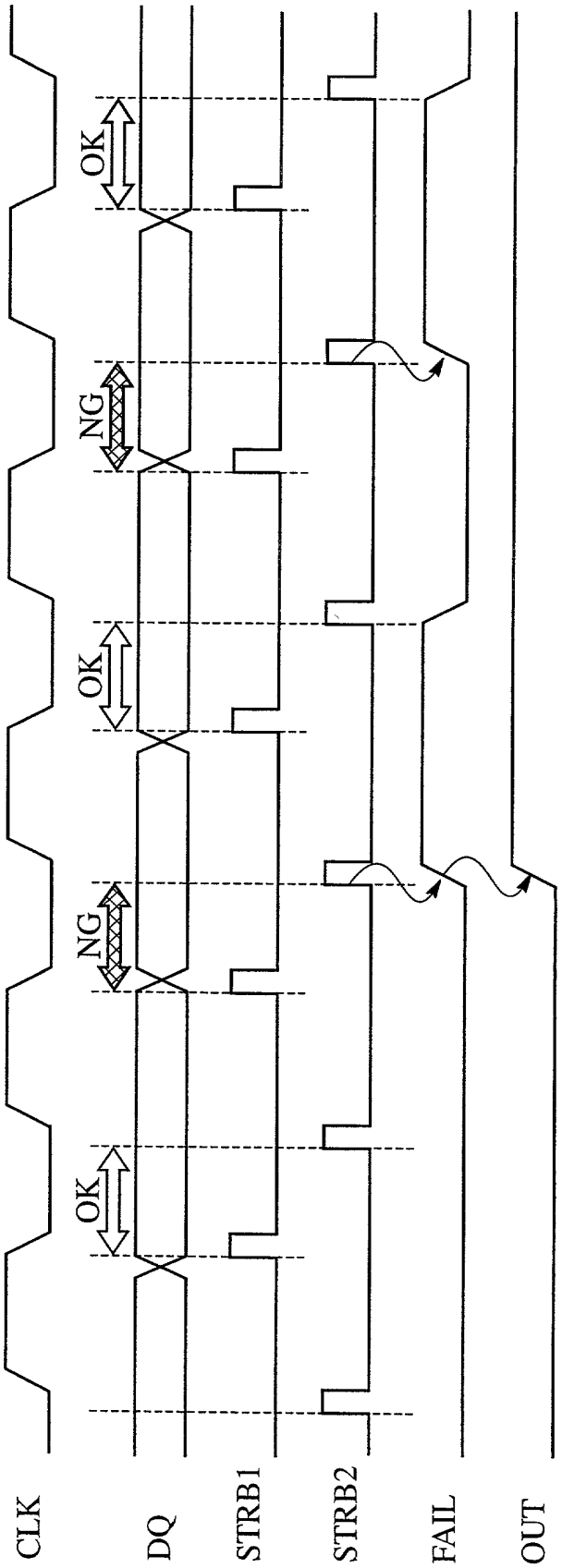

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FIG.7

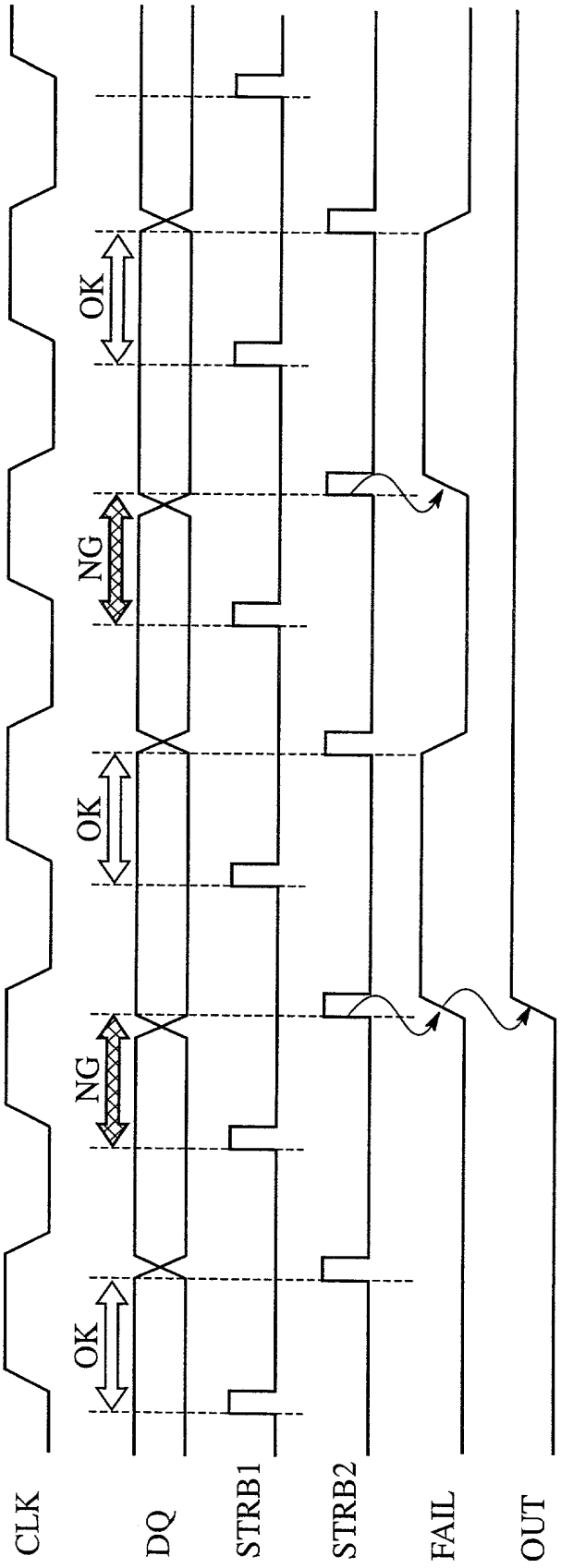

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FIG.8

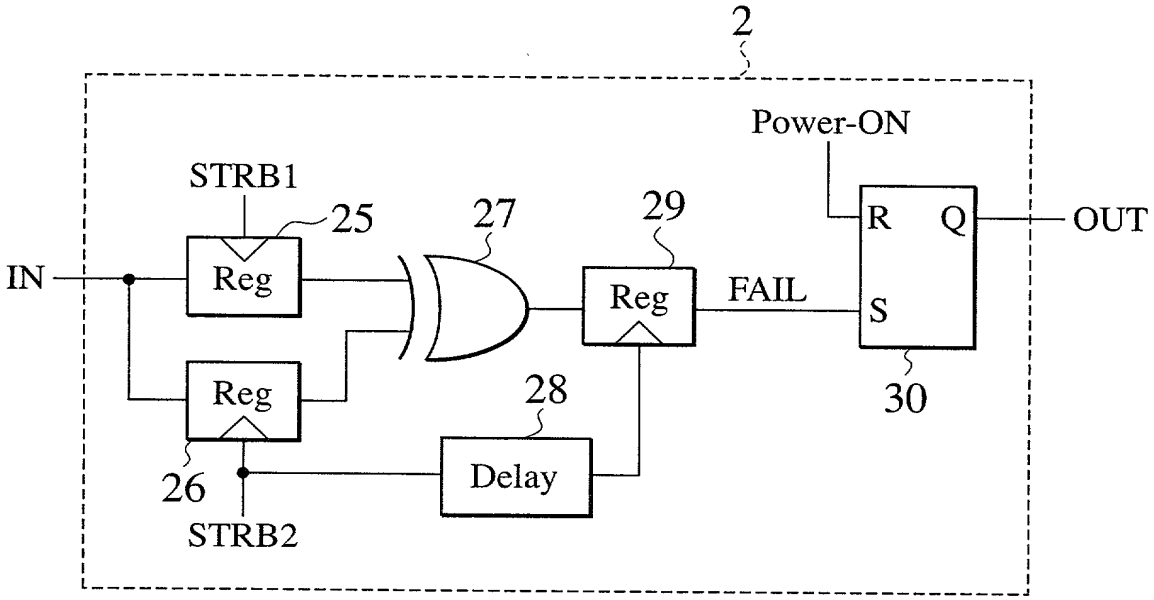
2
Power-ON
STRB1
25
27
29
R
Q
OUT
IN
Reg
Reg
FAIL
S
Reg
28
30
Delay
26
STRB2

FIG.9

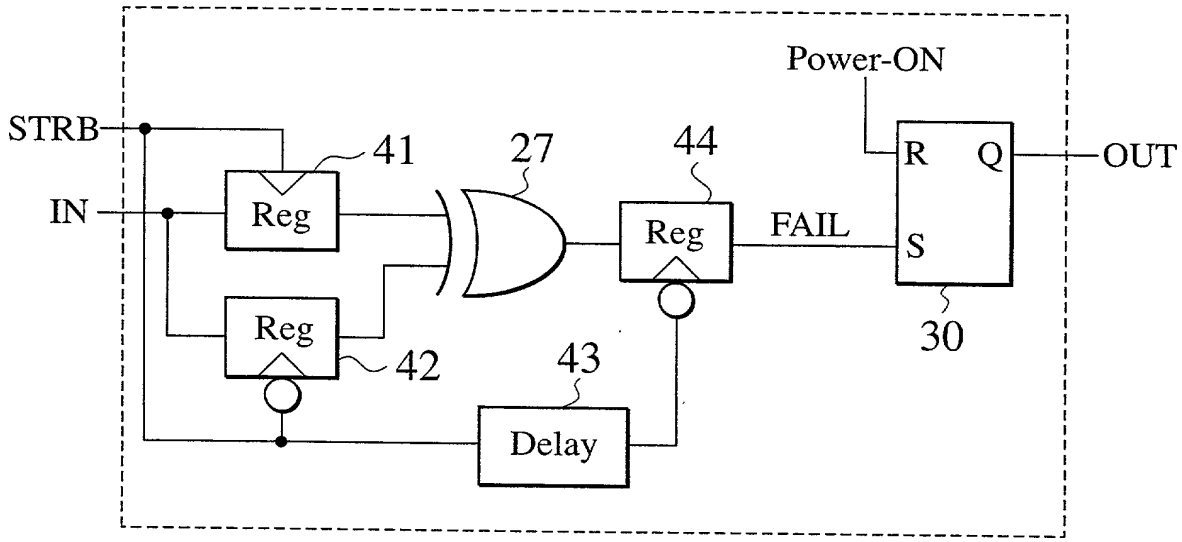
Power-ON
STRB
41
27
44
R
Q
OUT
IN
Reg
Reg
FAIL
S
Reg
30
42
43
Delay

FIG.10

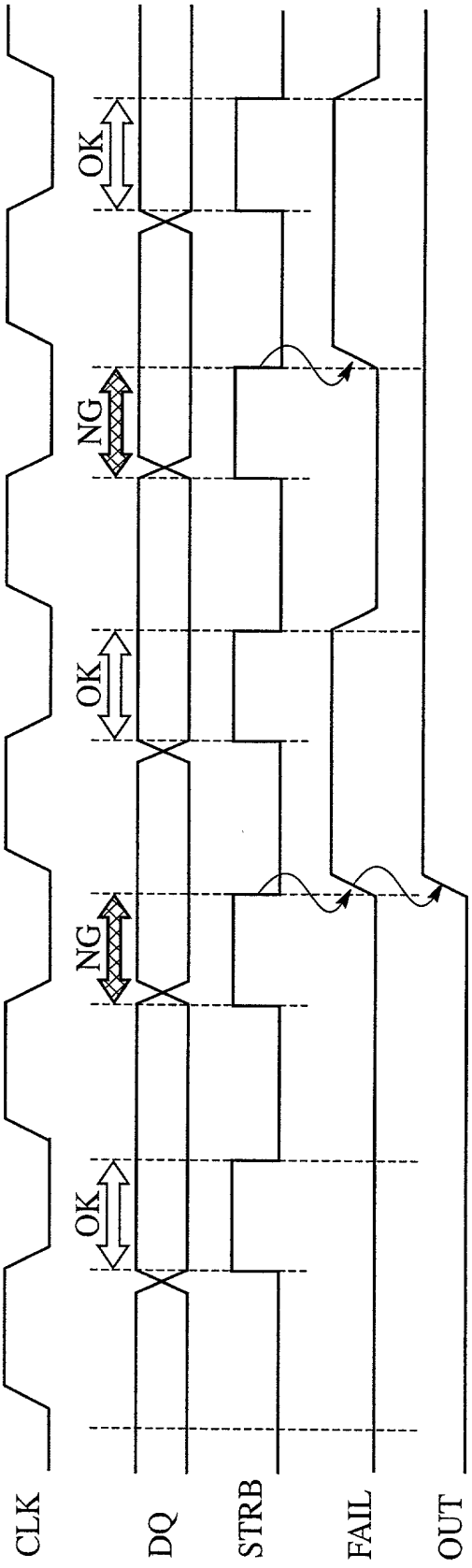

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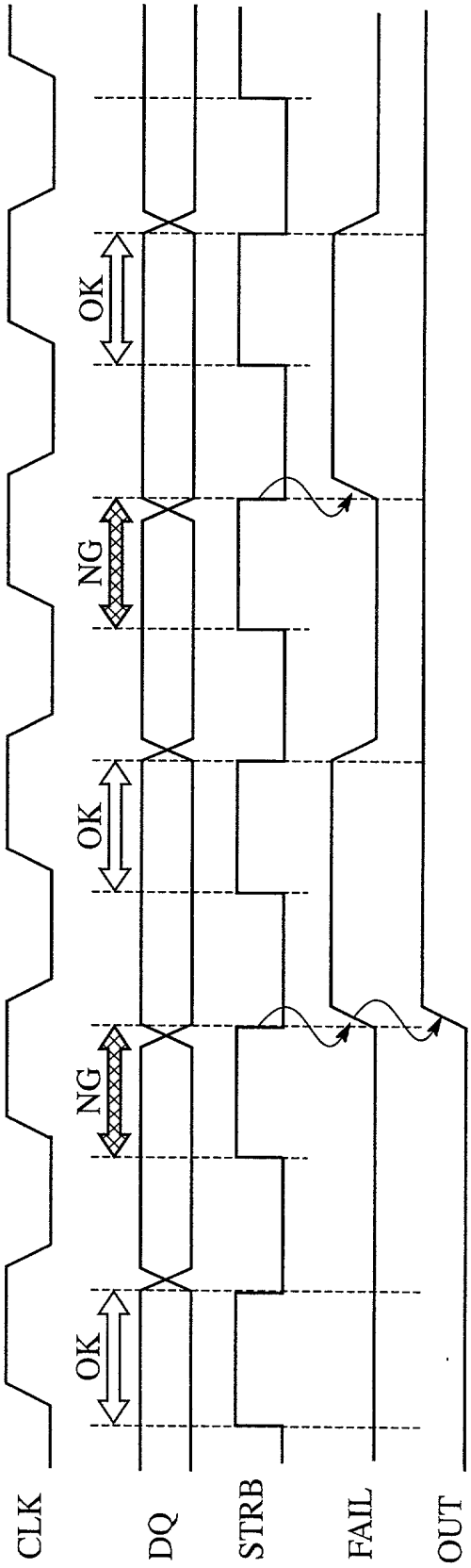
FIG.11



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